Motherboard Chipsets

- Provided by CPU manufacturer (Intel, AMD, etc)
- Provide integration of several common functions
  - Cache Controller
  - PCI Bus Interface
  - Dram Controller
  - Bridges to other busses
    + ISA, USB, etc.
- Used to be provided by third party vendors but these could not keep up with complexity of new CPUs, also hard to make time to market goals.

Typical PCI Based x86 Computer Architecture
AMD Motherboard

Note that communication between chips in chipset is via PCI bus.

Pentium II Motherboard with Intel 440LX Chipset

Note that communication between chips in chipset is via PCI bus.
INTEL 440LX AGPSET: 82443LX PCI
A.G.P. CONTROLLER (PAC)

- Supports the Pentium III Processor at 72 MHz
  - Supports 32-bit Addressing
  - Optimized In-Order and Request Queuing
  - Full Symmetric Multi-Processor (SMP) Protocol for up to Two Processors
  - Dynamic Deferred Transaction Support
  - GTL+ Compliant Host Bus
  - Supports WC Cycles
- Integrated DRAM Controller
  - EDO (Extended Data Out), and
  - Synchronous DRAM Support
  - Supports a Maximum Memory Size of 512 MB with SDRAM, or 1 GB
    with EDO
  - 6472-bit Path to Memory
  - Configurable DRAM Interface
  - Support for Auto Detection of Memory Type (SIMM Serial Presence Detect)
  - 8 RAS Lines Available
  - Support for 4-, 16- and 64-Mbit DRAM devices
  - Support for Symmetrical and Asymmetrical DRAM Addressing
  - Configurable Support for ECC/EC
  - ECC With Single Bit Error Correction and Multiple Bit Error Detection
  - Read-Around-Write Support for Host and PCI DRAM Read Accesses
  - Supports 3.3V DRAMs
- Accelerated Graphics Port (AGP) Interface
  - AGP Specification Compliant
  - AGP 66/133 MHz 3.3V Devices Supported
  - Synchronous Coupling to the Host Bus Frequency
- PCI Bus Interface
  - PCI Revision 2.1 Interface
  - Compliant
  - Greater Than 100-Mbps Data Streaming for PCI-to-SDRAM Accesses
  - Integrated Arbitration With Multi-Transaction PCI Arbitration
  - Acceleration Hooks
  - Five PCI Bus Masters Are Supported in Addition to the Host and PCI-to-
    ISA IO Bridge
  - Delayed Transaction Support
  - PCI Perity Checking and Generation Support
- Data Buffering For Increased Performance
  - Extensive CPU-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM Write Data Buffering
  - Write Combining Support for CPU-to-PCI Burst Writes
  - Supports Concurrent Host, PCI, and A.G.P. Transactions to Main Memory
- System Management Mode (SMM) Compliant
- 492 Pin BGA Package

INTEL 820 Chipset (for Pentium III)

82801AA ICH functions and capabilities include:
- PCI Rev 2.2 compliant with support for 33 MHz PCI operations
- Supports up to 6 Req/Gnt pairs (PCI Slots)
- Power Management Logic Support
- Enhanced DMA Controller, Interrupt Controller and Timer Functions
- Integrated IDE controller; Ultra ATA/66
- USB host interface with support for 2 USB ports
- System Management Bus (SMBus) compatible with most I²C devices
- AC'97 2.1 Compliant Link for Audio and Telephony CODECs
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Alert on LAN*
I82802 Firmware Hub

- Optional component for all 810 and above chipsets
- 4 or 8 Mbits of flash memory for non-volatile storage (can be used by BIOS)
- Contains a Random number generator based on thermal noise
  - Actual RNG instead of pseudorNG can increase security of encryption algorithms
Low Pin Count (LPC) interface

- Intended to be new interface between legacy devices (ISA, X-bus) and chipset
- Devices that interface with chipset thru LPC interface:
  - SuperIO devices (Keyboard, Serial Port, parallel port, Floppy Disk Controller)
  - Generic memory (BIOS)
- Uses PCI 33 Mhz clock
- Goal is a PC without either X-Bus or ISA

Intel 815E Chipset

- Intended for low cost to midstream PCs
- 3D graphics controller (low-performance, based on i740 3D graphics chip) integrated on chipset!
- SDRAM controller
- 2 USB controllers
- AGP port also included – if on-chip 3D controller is used, then AGP port used for texture cache
- LAN controller integrated (10/100 Mbit ethernet)
- All of the other usual stuff
815E block diagram

AGP port can support an external 3D video card

810 Chipset, cheaper version of 815.

No AGP port, intended for low cost PCs.
AGP - Advanced Graphics Port

- A dedicated, bi-directional, point-to-point bus meant for high speed transfers between the graphics adapter and system memory.
- Major problem with graphics card is memory:
  - Often need a lot of it (> 8Mb)
  - If this memory is placed on graphics card, then card is expensive.
  - If System memory is used, then access over PCI bus is slow
    + Solution, Add new dedicated bus!!!

AGP Data Paths

- Figure 1: Data Movement Paths and Corresponding AGP Modes.
Key Features of AGP

- Allows dual edge clocking on 66 Mhz bus
  - Data transferred on BOTH edges of clock (called 2X AGP)
  - Data bandwidth is 4 bytes * 133 Mhz = 533 MB/s
  - AGP 2.0 added 4X mode to increase bandwidth to 1066 MBs
- Implements sideband addressing for transaction commands
  - Separate command bus for transaction commands
  - Can queue up multiple transactions via command bus, data transfer on data bus is continuous as one transaction finishes and another begins.
Effect of Sideband Command Capability

SBA port is a separate port (8 bits) that contains just command data. Does not have to be used, main data bus can be used to pass all commands/data-addresses.

AGP 2X Transfer -- AD_STBx is driven by chipset

Figure 6: Multiple Outstanding Transactions

Figure 3-25: 2x Read Data - No Delay
Characteristics of High Performance Busses

- Wider is better (at least 32-bit data width)
- Dual edge clocking
- Split Transactions (issue a command to IO device to start transfer), then come back later when data is ready
- Bus Mastership
- Advanced Signaling
  - Limited voltage swing, differential signaling
Pentium II/III GTL Bus (Host Bus)

- Gunning Transceiver Logic (GTL) used for Pentium II local bus (66Mhz now, 100Mhz, 133 Mhz)
  - GTL bus is open drain bus where all runs are terminated
  - Termination voltage (Vtt) is 1.5 v.
- GTL bus is a differential bus with only wire!
  - Vref used by all receivers, drivers
    + Vref (1.0v) is 2/3 of Vtt.
  - Voltage swing about Vref is +/- 200 mv.
    + Less voltage swing => higher speed, less noise margin

GTL Bus (continued)

- Interconnections on a GTL bus are transmission lines so interconnect topology, termination very important.
- Interconnection is point to point to avoid stubs (stubs generate reflections)